08 423402

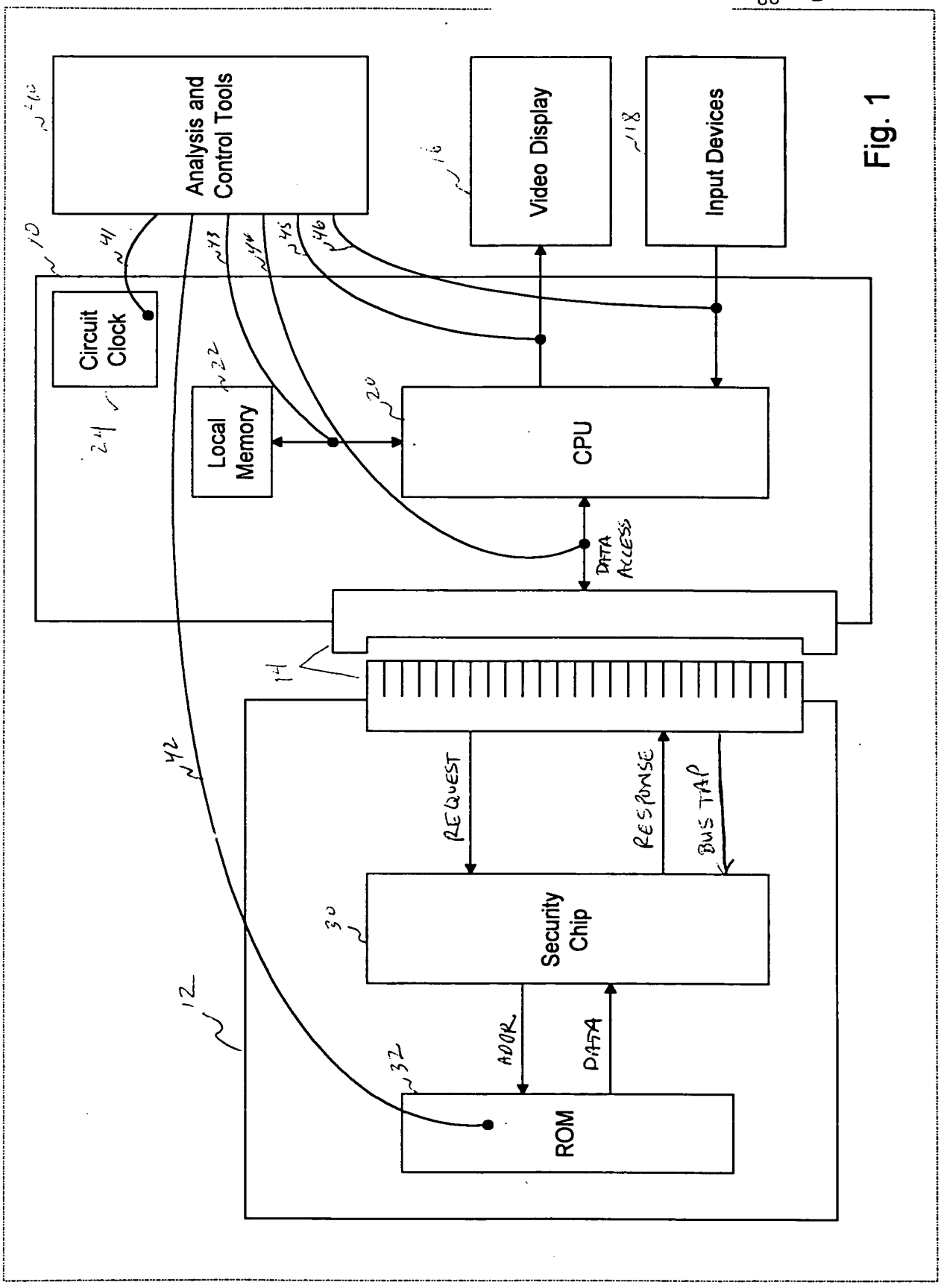

Fig. 1

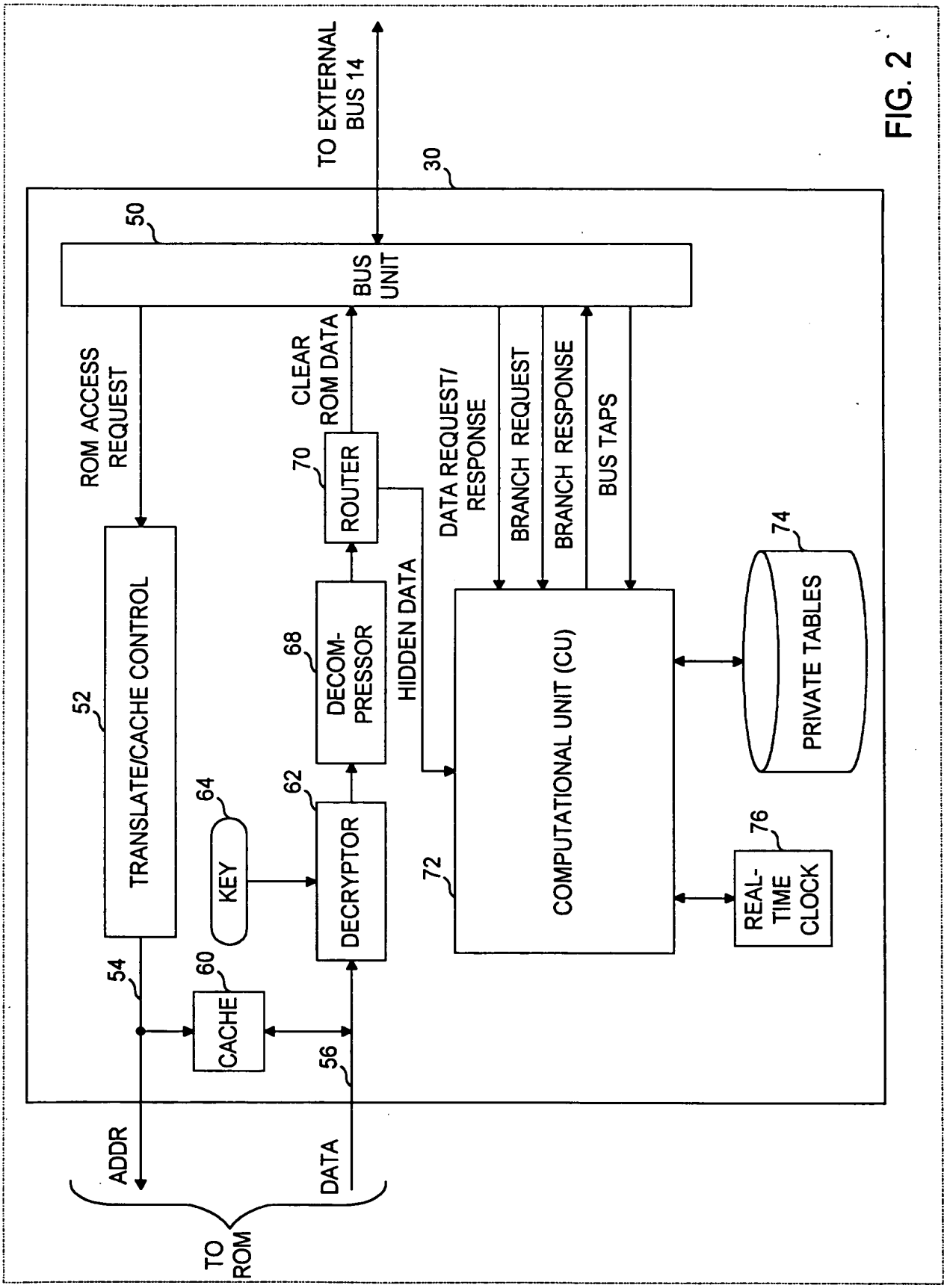
TO EXTERNAL BUS 14
30
50
BUS UNIT
ROM ACCESS REQUEST
CLEAR ROM DATA
70
ROUTER
DATA REQUEST/ RESPONSE
BRANCH REQUEST
BRANCH RESPONSE
BUS TAPS
74
PRIVATE TABLES
52
TRANSLATE/CACHE CONTROL
68
DECOM-PRESSOR
HIDDEN DATA
COMPUTATIONAL UNIT (CU)
64
KEY
62
DECRYPTOR
72
76
REAL-TIME CLOCK
54
60
CACHE
56
ADDR
DATA
TO ROM

FIG. 2

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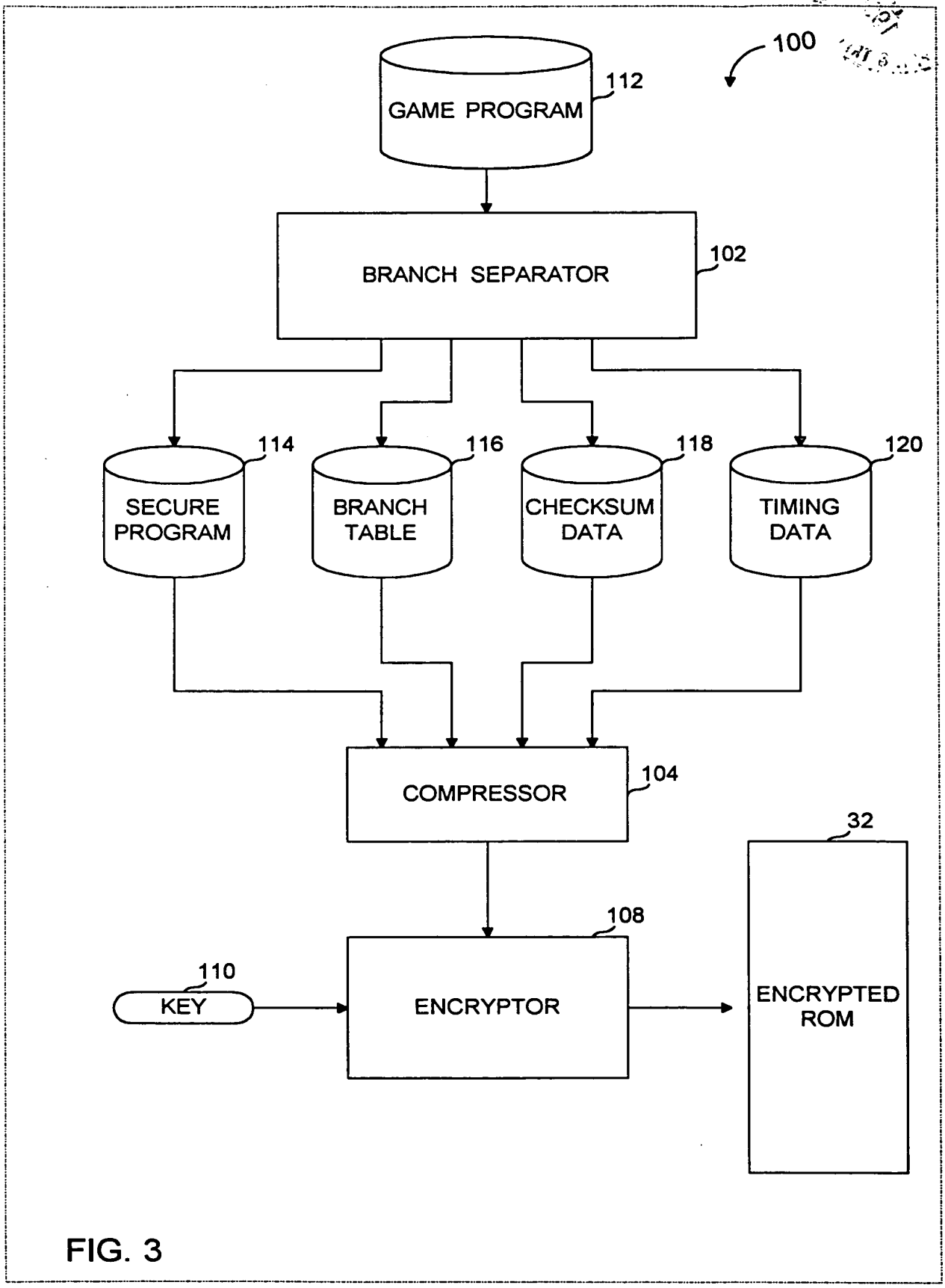

FIG. 3

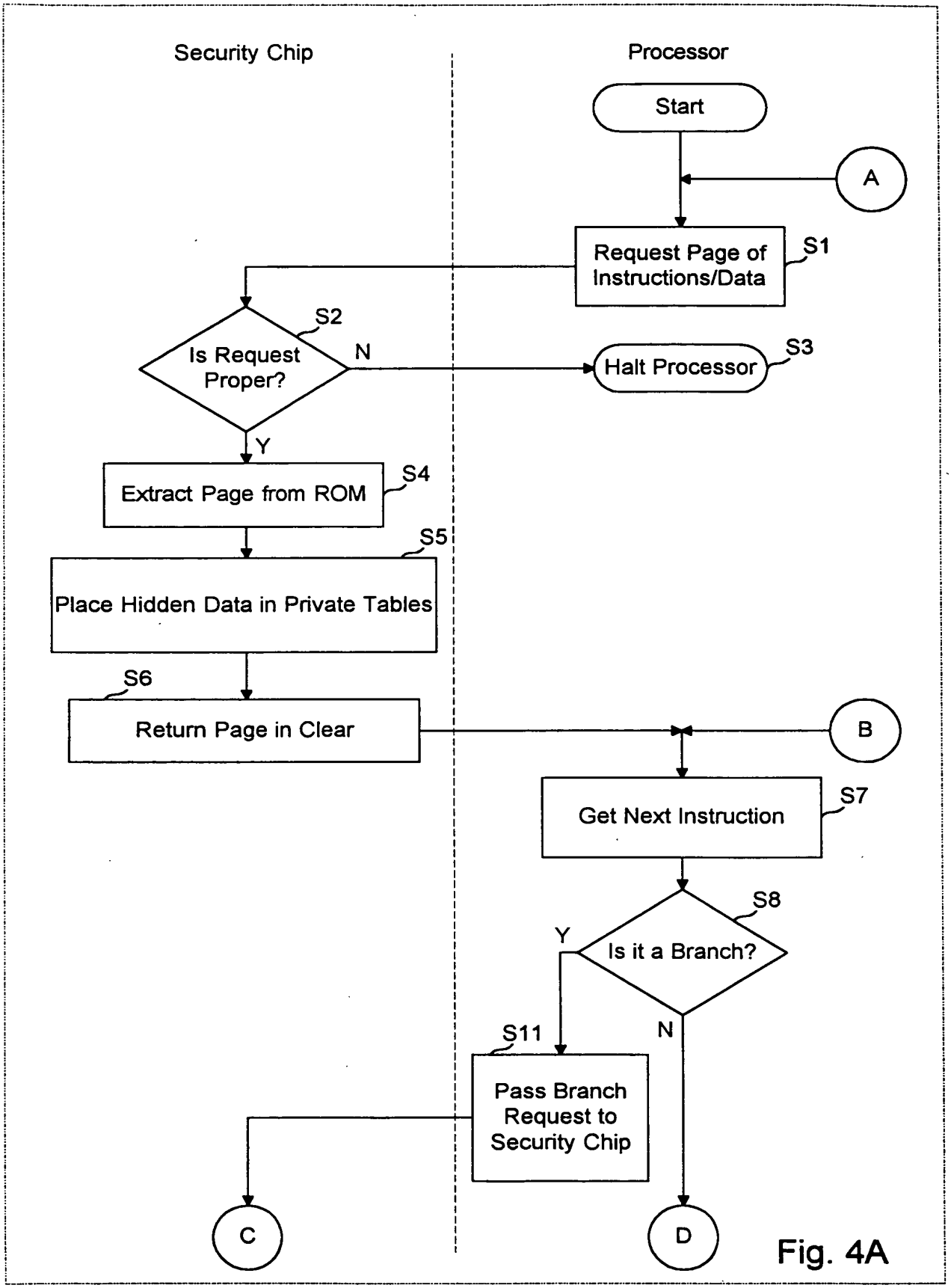
Security Chip
Processor
Start
A
Request Page of Instructions/Data
S1
S2
Is Request Proper?
N
Halt Processor
S3
Y
Extract Page from ROM
S4
S5
Place Hidden Data in Private Tables
S6
Return Page in Clear
B
Get Next Instruction
S7
S8
Y
Is it a Branch?
N
S11
Pass Branch Request to Security Chip
C
D

Fig. 4A

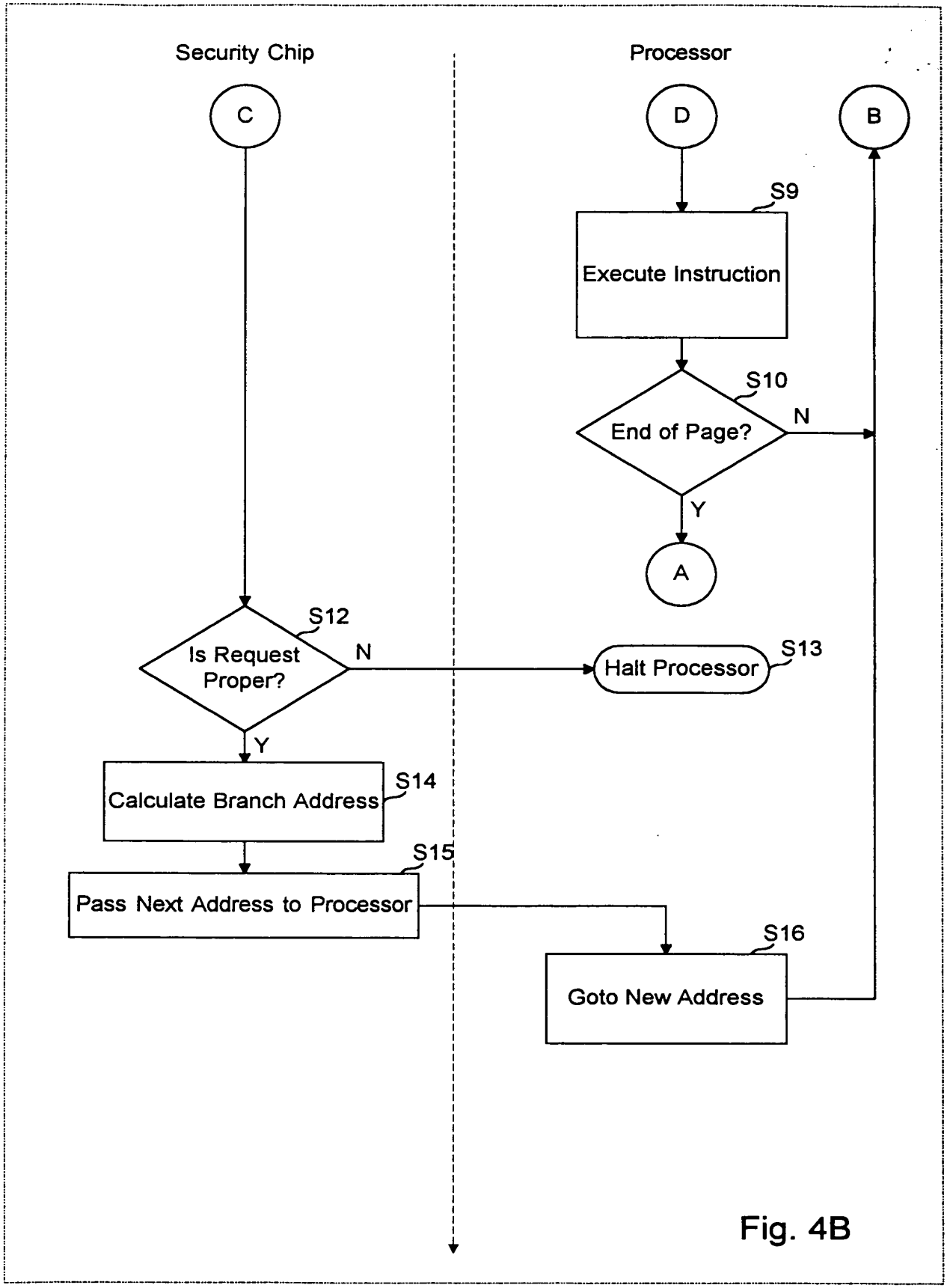
Security Chip
Processor
C
D
B
S9
Execute Instruction
S10
End of Page?
N
Y
A
S12
Is Request Proper?
N
S13
Halt Processor
Y
S14
Calculate Branch Address
S15
Pass Next Address to Processor
S16
Goto New Address

Fig. 4B

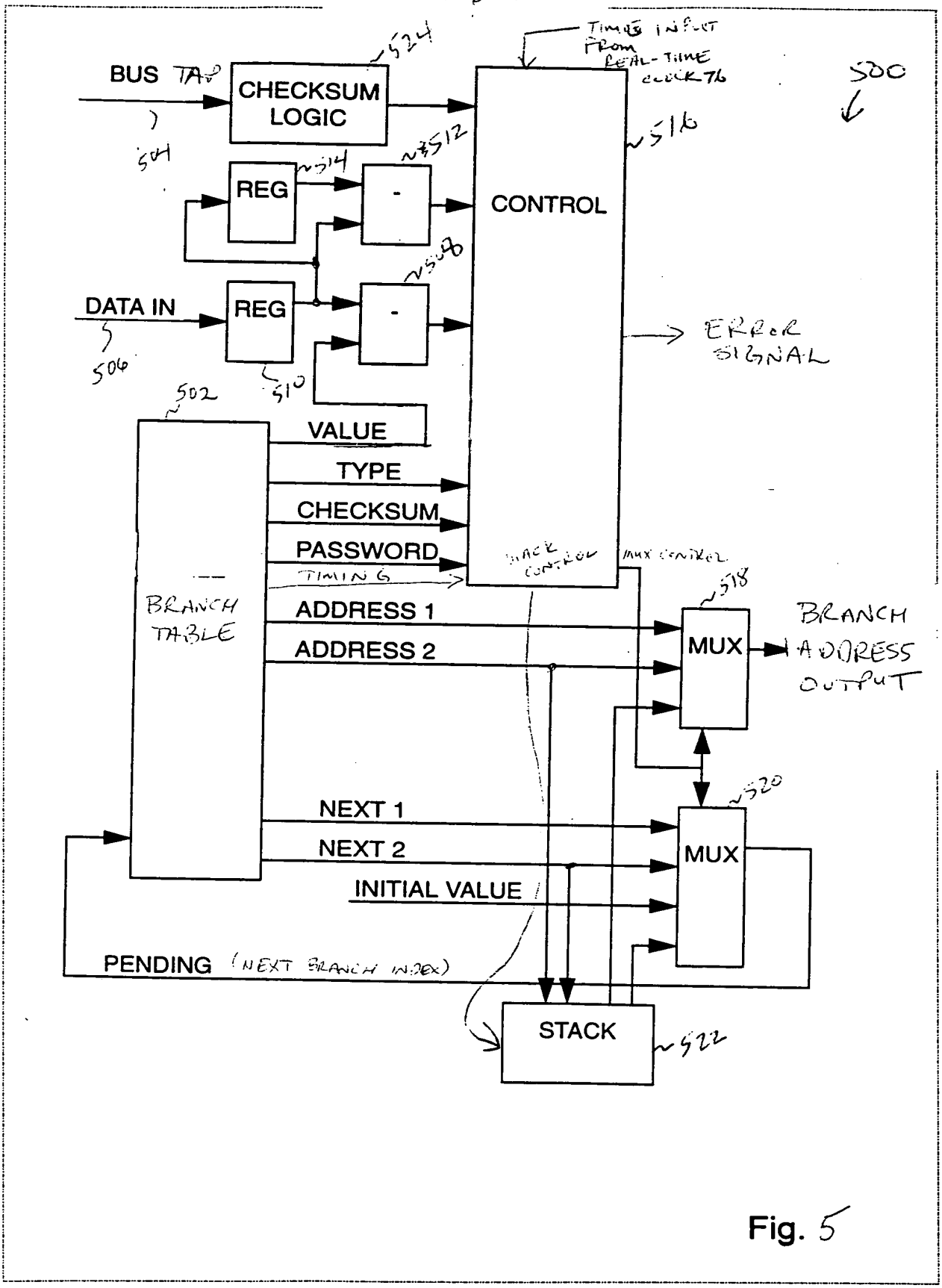
BUS TAP
504
CHECKSUM LOGIC
524
TIMER INPUT FROM REAL-TIME CLOCK 76
500
516
REG
514
512
CONTROL
DATA IN
506
REG
510
526
ERROR SIGNAL
502
VALUE
TYPE
CHECKSUM
PASSWORD
TIMING
BRANCH TABLE
STACK CONTROL
MUX CONTROL
518
ADDRESS 1
ADDRESS 2
MUX
BRANCH ADDRESS OUTPUT
520
NEXT 1
NEXT 2
INITIAL VALUE
MUX
PENDING (NEXT BRANCH INDEX)
STACK
522

Fig. 5

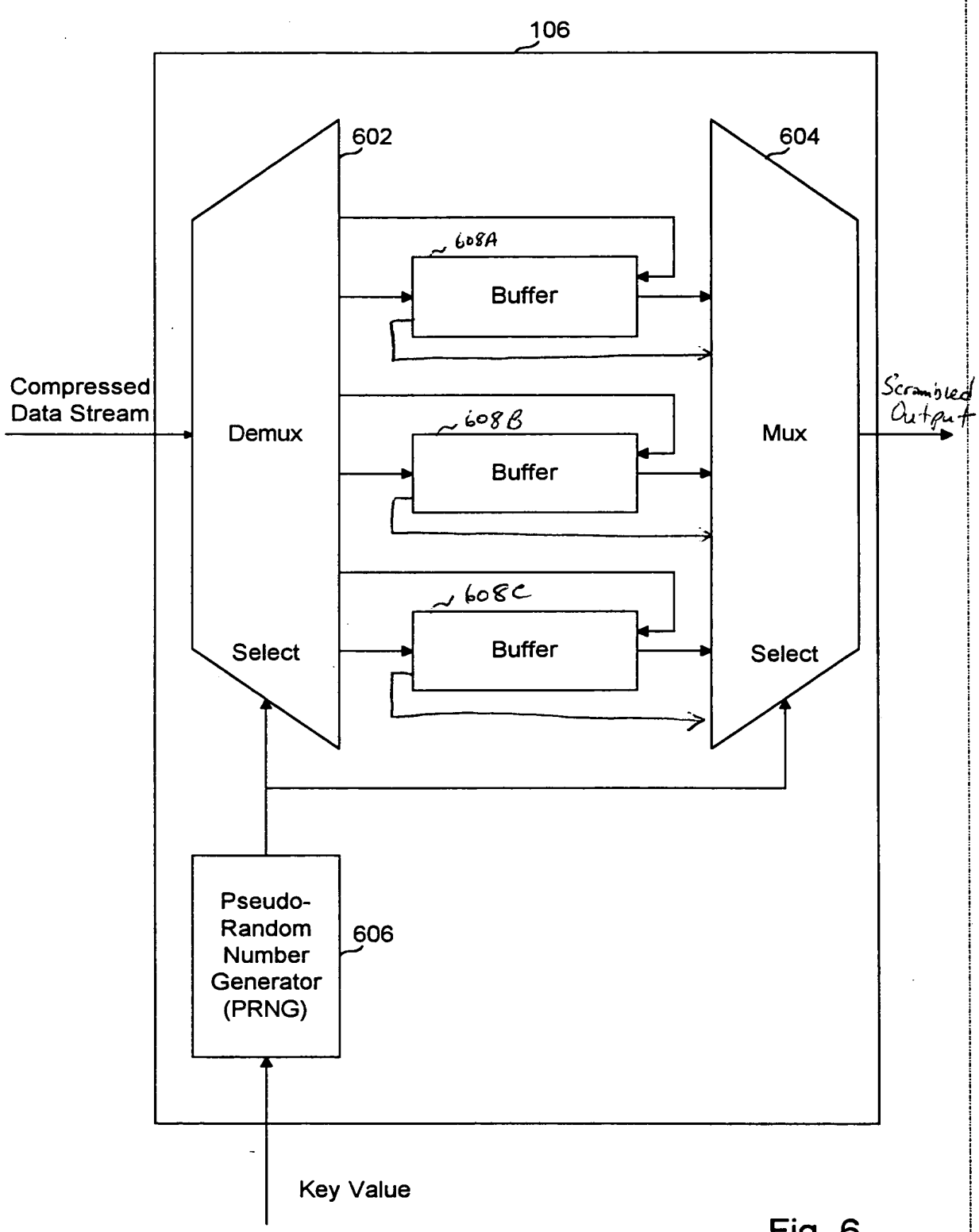
106
602
604
608A
Buffer
608B
Buffer
608C
Buffer
Compressed Data Stream
Demux
Mux
Scrambled Output
Select
Select
Pseudo-Random Number Generator (PRNG)
606
Key Value

Fig. 6

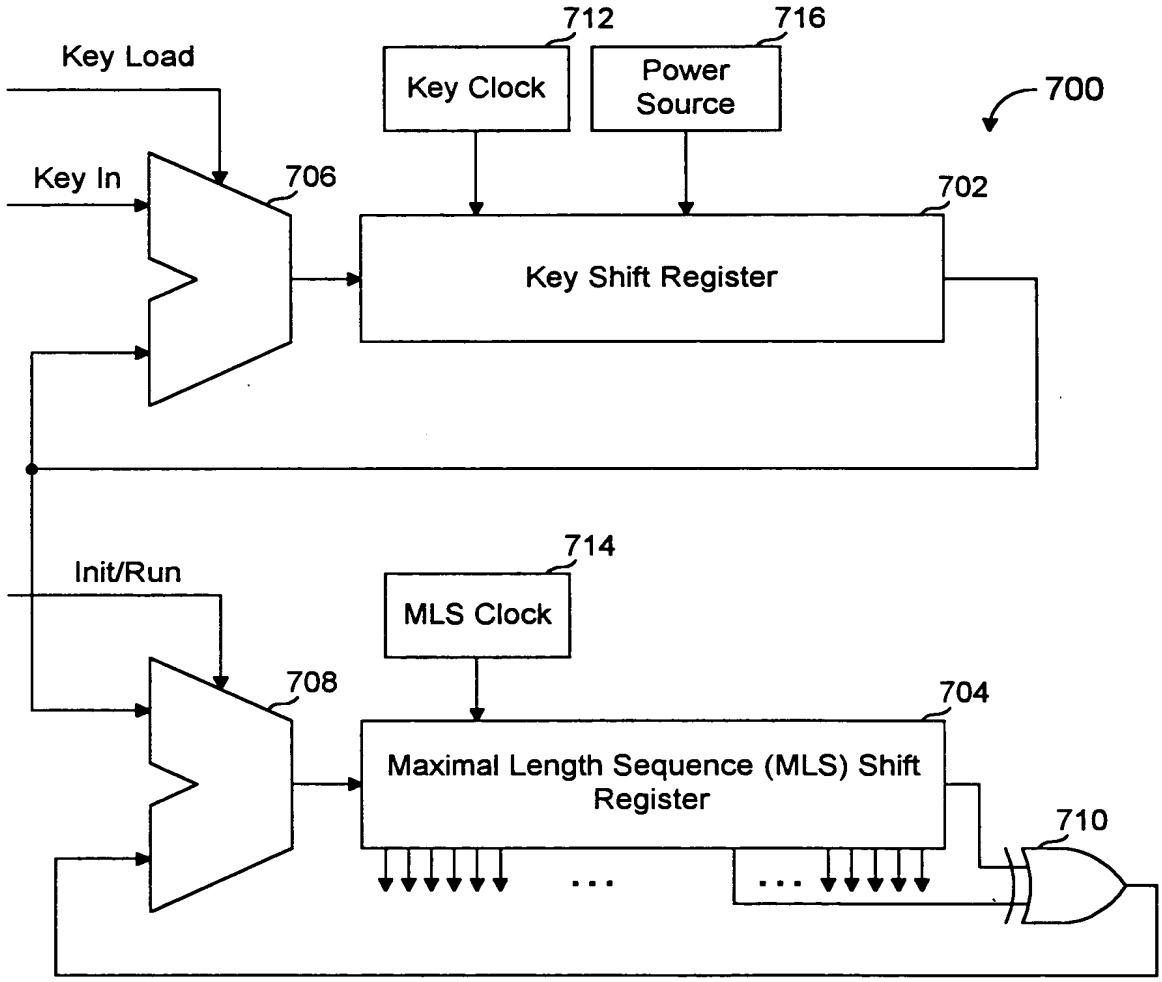
712
716
Key Load
Key Clock
Power Source
700
Key In
706
702
Key Shift Register
714
Init/Run
MLS Clock
708
704
Maximal Length Sequence (MLS) Shift Register
710

Fig. 7